

What is claimed is:

1. A non-volatile memory device comprising:
address input connections to receive externally provided signals; and
control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the externally provided signals.
2. The non-volatile memory device of claim 1 further comprising a test mode latch circuit.
3. The non-volatile memory device of claim 2 wherein the control circuitry initiates a test operation in response to externally provided commands when the test mode latch is in a first state.
4. The non-volatile memory device of claim 2 wherein the control circuitry initiates a test operation in response to externally provided commands and an electronic key when the test mode latch is in a second state.
5. The non-volatile memory device of claim 4 wherein the electronic key comprises a voltage detection circuit coupled to an external input connection to detect an elevated voltage applied to the external input connection.
6. The non-volatile memory device of claim 5 wherein the external input connection is one of the address input connections.
7. A flash memory device comprising:
an array of non-volatile memory cells;
control input connections to receive control signals;
data connections for bi-directional data communication;

address input connections to receive externally provided address and test mode code signals; and

control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals.

8. The flash memory device of claim 7 further comprises a test mode latch circuit.

9. The flash memory device of claim 8 wherein the control circuitry initiates a test operation in response to externally provided commands when the test mode latch is in a first state.

10. The flash memory device of claim 8 wherein the control circuitry initiates a test operation in response to externally provided commands and an electronic key circuit when the test mode latch is in a second state.

11. The flash memory device of claim 10 wherein the electronic key circuit comprises a voltage detection circuit coupled to an external input connection to detect an elevated voltage applied to the external input connection.

12. The flash memory device of claim 11 wherein the external input connection is one of the address input connections.

13. A memory system comprising:
an external memory controller; and
a flash memory device coupled to the external memory controller, the flash memory device comprises,
an array of non-volatile memory cells,
control input connections to receive control signals from the external memory controller,

data connections for bi-directional data communication with the external memory controller,

address input connections to receive externally provided address and test mode code signals from the external memory controller, and

control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals.

14. The memory system of claim 13 wherein the flash memory device further comprises a test mode latch circuit, wherein the control circuitry initiates a test operation in response to externally provided commands when the test mode latch is in a first state, and wherein the control circuitry initiates a test operation in response to externally provided commands and an electronic key circuit when the test mode latch is in a second state.

15. The memory system of claim 14 wherein the electronic key circuit comprises a voltage detection circuit coupled to one of the address input connections to detect an elevated voltage applied to the one of the address input connections.

16. A method of testing a non-volatile memory device comprising:
initiating a test operation of the non-volatile memory device; and
selecting a test mode in response to a test code provided on address inputs.

17. The method of claim 16 wherein initiating the test operation comprises:
receiving test mode commands on the address inputs; and
placing the non-volatile memory device in a test mode.

18. The method of claim 17 further comprises checking a state of a test latch circuit prior to placing the non-volatile memory device in the test mode.

19. The method of claim 18 wherein the non-volatile memory device is prohibited from being placed in the test mode if the test latch circuit is in a first state.

20. The method of claim 16 wherein initiating the test operation comprises:
checking a state of a test latch circuit;
receiving test mode commands on the address inputs; and
placing the non-volatile memory device in a test mode if the test latch circuit is in a first state, and prohibiting the test mode if the test latch circuit is in a second state.

21. The method of claim 20 further comprises:
placing the non-volatile memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined address input.

22. A method of testing a non-volatile memory device comprising:
checking a state of a test latch circuit;
receiving test mode commands on address inputs;
placing the non-volatile memory device in a test mode if the test latch circuit is in a first state, and prohibiting the test mode if the test latch circuit is in a second state;
and
selecting a test mode in response to a test code provided on the address inputs.

23. The method of claim 22 wherein the test latch circuit comprises a non-volatile memory cell.

24. The method of claim 22 further comprises placing the non-volatile memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined address input.

25. A method of operating a non-volatile memory device comprising:

performing a first Load Command Register operation, wherein the first Load Command Register operation comprises receiving a test mode command on address input connections when a chip select input is active, a row access strobe input is active, a column access strobe input is active and a write enable input is inactive, wherein the test mode command initiates a test mode; and

performing a second Load Command Register operation, wherein the second Load Command Register operation comprises receiving a test code command on address input connections when a chip select input is active, a row access strobe input is active, a column access strobe input is active and a write enable input is inactive, wherein the test code command instructs the memory device to perform a selected test operation.

26. The method of claim 25 further comprises:

checking a state of a test latch circuit; and

placing the non-volatile memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined one of the address input connections.

27. A method of testing a non-volatile memory device comprising:

checking a state of a non-volatile test latch circuit;

receiving test mode commands on address inputs;

placing the non-volatile memory device in a test mode if the test latch circuit is in a first state, ^{or} ~~and prohibiting the test mode~~ if the test latch circuit is in a second state;

placing the non-volatile memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined address input; and

selecting a test mode in response to a test code provided on the address inputs.

28. A method of testing a memory device having X selectable tests, the method comprises:

initiating a test mode; and

selecting one of the X selectable tests using a test code provided on address input connections.

29. The method of claim 28 wherein initiating the test mode comprises:
receiving test mode commands on the address input connections; and
placing the memory device in the test mode.

30. The method of claim 29 further comprises checking a state of a test latch circuit prior to placing the memory device in the test mode.

31. The method of claim 30 wherein the memory device is prohibited from being placed in the test mode if the test latch circuit is in a first state.

32. The method of claim 28 wherein initiating the test mode comprises:
checking a state of a test latch circuit;
receiving test mode commands on the address input connections; and
placing the memory device in a test mode if the test latch circuit is in a first state, and prohibiting the test mode if the test latch circuit is in a second state.

33. The method of claim 32 further comprises:
placing the memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined address input.

34. A flash memory device comprising:
an array of non-volatile memory cells;
control input connections to receive control signals;

X-data connections for bi-directional data communication;
address input connections to receive externally provided address; and
control circuitry to place the memory in a compressed data mode such that X-
bits of data are communicated using X/Y data connections, and wherein the control
circuitry is coupled to the address input connections to place the non-volatile memory
device in a test mode selected by test mode code signals.

35. The flash memory device of claim 34 further comprises a test mode latch circuit,
and the control circuitry initiates a test operation in response to externally provided
commands when the test mode latch is in a first state.

36. The flash memory device of claim 34 further comprises a test mode latch circuit,
and the control circuitry initiates a test operation in response to externally provided
commands and an electronic key circuit when the test mode latch is in a second state.

37. The flash memory device of claim 36 wherein the electronic key circuit
comprises a voltage detection circuit coupled to an external input connection to detect
an elevated voltage applied to the external input connection.

38. A method of testing a non-volatile memory device comprising:
placing the non-volatile memory in a compressed data mode such that X-bits of
data are communicated on X/Y data connections;
checking a state of a test latch circuit;
receiving test mode commands on address inputs;
placing the non-volatile memory device in a test mode if the test latch circuit is
in a first state, and prohibiting the test mode if the test latch circuit is in a second state;
and
selecting a test mode in response to a test code provided on the address inputs.

39. The method of claim 38 wherein the test latch circuit comprises a non-volatile memory cell.

40. The method of claim 39 further comprises placing the non-volatile memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined address input.

41. A method of testing a non-volatile memory device comprising:

placing the non-volatile memory in a compressed data mode such that X-bits of data are communicated on X/Y data connections;

checking a state of a non-volatile test latch circuit;

receiving test mode commands on address inputs;

placing the non-volatile memory device in a test mode if the test latch circuit is in a first state, and prohibiting the test mode if the test latch circuit is in a second state;

placing the non-volatile memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined address input; and

selecting a test mode in response to a test code provided on the address inputs.